University of Denver
Department of Electrical and Computer Engineering

ENCE 3100
Advanced Digital Systems Design

Class	**MWF**	**12:00-12:50 p.m.**	**CMK-201**
Laboratory	**T**	**10:00-12:50 p.m.**	**CMK-301**

Instructor: **Dr. Mohammad H. Mahoor**
Office: **CMK 306, Phone: (303) 871-3745**
E-Mail: **mmahoor@du.edu**

Office Hours: **MW 2:00-4:00p.m., and by appointment**
Pre/Co-requisites: ENCE 2101 - Digital Design

Course Texts:

1. Donald D. Givone, *Digital Principles and Design*, copyright 2003 McGraw-Hill, ISBN 0-07-252503-7 **[REQUIRED]**
2. M. Morris Mano and Michael D. Ciletti, Digital Design, 4th Edition 2007 PEARSON Prentice Hall, ISBN 0-13-198924-3. [Recommended]
3. William W. Hines, Douglas C. Montgomery, David M. Goldsman, Connie M. Borror, Probability and Statistics in Engineering , 4th Edition ISBN: 978-0-471-24087-7, January 2003 **[REQUIRED]**
4. Alberto Leon-Garcia, Probability, Statistics, and Random Processes For Electrical Engineering (3rd Edition), Publisher: Prentice Hall; 3 edition (January 7, 2008) ISBN-10: 0131471228 [Recommended]

Course Description

Part 1:

This course is the continuation of Digital Design (ENCE-2101). Topics covered will focus on the design of digital systems using combinational, sequential, and programmable logic devices. Techniques for logic design including asynchronous logic, physical world interfaces to digital systems, and system performance analysis methods will be studied.

Part 2:

An introduction to probability and statistics will be covered.

Course Objectives:

- To learn and apply design, synthesis, and analysis methods for digital systems that incorporate MSI/VLSI devices (e.g. counters, shift registers, and ALUs).
- To learn and apply methods to analyze the timing behavior and to detect timing hazards in digital circuits.
- To learn methods for analysis and design of sequential digital circuits with feedback.

- To learn and apply design, synthesis, and analysis methods of digital systems that incorporate programmable logic devices (PLDs).
- To understand probability and statistical methods and the application of these principles in electrical engineering.

Grading

Homework. …….. 25%
Midterm Examinations (2). ……. …… . 20% (10% each)
Final Examinations.. …….. 15%
Laboratory. …….. 40 %

Homework: All Homework assignments are due at the BEGINNING of the class session. **No late homework will be accepted.** In special cases due to excused absence, assignments will be accepted with an applied reduction in grade. Students are responsible for the written clarity of their homework assignments. No credit will be given to homework problems which cannot be read or understood.
Grading issues can be resolved by, coming in during office hours and explaining the solution OR attach a note, which explains the solution, to the graded assignment and returning it.

Examinations: Two 50-minute examinations will be given during the semester; and a final exam will be given during exam week at the end of the quarter. The tests are comprehensive, closed book and closed notes. If for any reason a student is unable to attend an exam, arrangements with the instructor must be made prior to the test. Examinations are scheduled on the following dates

Midterm #1: October 6, 2008 (Monday)
Midterm #2: November 3, 2008 (Monday)
Final: November 17, 2008 (Monday) 12:00-1:50 p.m.

Laboratory: There are approximately 5 laboratory assignments and 1 final project. Students must work individually on their laboratory assignment/project. Each student is responsible for submitting a report documenting his or hers activities. The report grade is base on clarity of presentation, accuracy of procedures and results, and correctness of procedures and results. (Note: Students are encouraged to help one another; but each student must do their own work and submit their own report.)

Course Software
The programmable logic devices (PLDs) used in the laboratory for this course are manufactured by Lattice Semiconductor Corporation. The software used for writing programs for programmable logic devices can be downloaded from the Lattice Semiconductor web site. Downloading a copy of the software is a 2-step process - download the software and getting a license to use the software. The following instructions help step you through the process:
(The isplever-Starter is installed and available on the PCs in the Lab. CMK-301)
1. Go to http://www.latticesemi.corm
2. Click on the **Download** heading.
3. Click on **Software.**
4. Click on **isplever-classic.**
5. Read and agree (Click Yes) to the license agreement; Click "Continue to download".
6. (Optionally you can download) **Starter Help and User Guides.**

Once the software is downloaded and installed, the software must be licensed for use. So from the menu on http://www.latticesemi.com

7. Click on **Support** heading, and then **licensing.**
8. Click on **isplever-classic.** Follow the directions for obtaining your license.

Tentative Course Outline
Simplification of Boolean Expressions: Chapter 4, Givone's text, (review)
Synchronous Counters: 6.8 - 6.9
Programmable Logic Devices (PLDs): 5.7 - 5.10
a. ABEL Programming Language
Circuit Timing: 6.3 - 6.4
Timing Hazards: 9.9 - 9.10
Synchronous Sequential Networks (Review): Chapter 7
Asynchronous Sequential Networks: 9 - 9.8
Algorithmic State Machines: Chapter 8

Probability: Chapter: Selections from chapters 1-2, 5 and 7, Hines's text

Honor Code
All members of the University community are entrusted with the responsibility of observing certain ethical goals and values as they relate to academic integrity. Essential to the fundamental purpose of the University is the commitment to the principles of truth and honesty. The Honor Code is designed so that responsibility for upholding these principles lies with the individual as well as the entire community.
The Honor Code fosters and advances an environment of ethical conduct in the academic community of the University, the foundation of which includes the pursuit of academic honesty and integrity. Through an atmosphere of mutual respect we enhance the value of our education and bring forth the highest standard of academic excellence. Members of the University community, including students, faculty, staff, administrators and trustees, must not commit any intentional misrepresentation or deception in academic or professional matters.